1600 MHz to 2600 MHz Quadrature Modulator with Integrated Fractional-N PLL and VCO

Preliminary Technical Data

ADRF6703

FEATURES

IQ Modulator with Integrated Fractional-N PLL
Output frequency range: 1600 MHz to 2600 MHz
Internal LO Frequency Range: 2100 MHz to 2600 MHz
Output P1dB: +16 dBm
Output IP3: +35 dBm
Noise Floor: -158 dBm/Hz
Baseband Modulation bandwidth: 500 MHz (3 dB)
SPI Serial Interface for PLL Programing
Power Supply: +5 V / 210 mA
40 Pin 6mm X 6mm LFCSP

GENERAL DESCRIPTION

The ADRF6703 is an IQ modulator with integrated PLL and VCO. The PLL/Synthesizer uses a Fractional-N PLL to generate a $2*F_{LO}$ input to the I-Q modulator. The PLL reference input is supported from 12MHz to 160MHz. The phase detector output controls a charge pump whose output is integrated in an off-chip loop-filter. The loop filter output is then applied to an integrated VCO. The VCO output at $2*F_{LO}$ is then applied to a quadrature divider as well as to a programmable divider. The programmable divider is controlled by a sigma-delta modulator (SDM). The I-Q modulator has analog I + Q inputs which can be at baseband or optionally at a complex IF up to 200 MHz

Table 1. Device Frequency Ranges

Part #	Internal LO Range	+/-3dB RF Out Balun Range	+/-1dB RF Out Balun Range
ADRF6701	750 MHz 1160 MHz	400 MHz 1300 MHz	550 MHz 1000 MHz
ADRF6702	1550 MHz 2150 MHz	1200 MHz 2400 MHz	1550 MHz 2200 MHz
ADRF6703	2100 MHz 2600 MHz	1600 MHz 2600 MHz	1900 MHz 2400 MHz
ADRF6704	2500 MHz 2900 MHz	2200MHz 3000MHz	2400 MHz 2800 MHz

The modulator mixes the I-Q inputs from the analog inputs with the quadrature LO from the quadrature divider. The differential output is converted to a single-ended output intended to drive a 50-Ohm load.

The device is fabricated using an advanced silicon-germanium BiCMOS. It is available in a 40-lead, exposed-paddle, Pb-free, 6mm x 6mm LFCSP package. Performance is specified over a −40°C to +85°C temperature range.

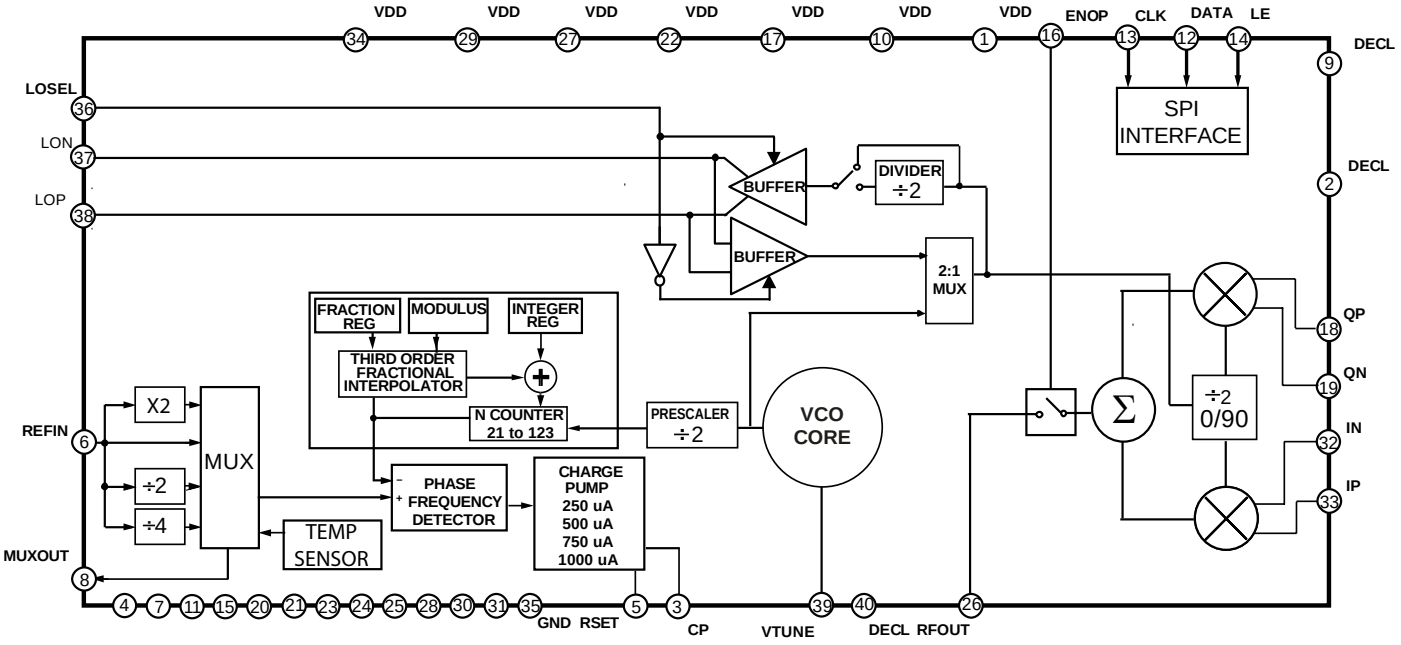

Figure 1. Block Diagram

Rev. PrF

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SPECIFICATIONS

VDD = 5 V; Ambient Temperature (T_A) = 25°C; I/Q inputs = 1 V p-p differential sine waves in quadrature on a 500 mV dc bias; f_{PFD}=38.4 MHz, f_{REF}= 153.6 MHz, Modulator Baseband Frequency = 1 MHz, Output Frequency = 2200 MHz unless otherwise noted.

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
RF OUTPUT	Pin RFOUT				
IQ ModulatorOperating Frequency Range		1600		2600	MHz
Internal LO Frequency Range		2100		2600	MHz
Nominal Output Power	Baseband VIQ= 1 Vpp differential		6		dBm
Output Harmonics	2nd Harmonic		-60		dBc
	3rd Harmonic		-58		dBc
Gain Flatness vs. Frequency	Pout=-7dBm, +/-40MHz		0.3		dB
OP1dB			16		dBm
OIP3	$F1_{BB}$ = 3.5 MHz, $F2_{BB}$ = 4.5 MHz, P_{OUT} = -5 dBm per tone		35		dBm
OIP2	$F1_{BB}$ = 3.5 MHz, $F2_{BB}$ = 4.5 MHz, P_{OUT} = -5 dBm per tone		72		dBm
Carrier Feedthrough	at LO Frequency/2		-38		dBm
Sideband Suppression			-42		dBc
Noise Floor	All inputs tied to 0.5 V		-158		dBm/Hz
LO INPUT/OUTPUT	LOP, LON				
Output Frequency Range	Divide by 2 bypass	2100		2600	MHz
LO Ouput Level	2*LO or 1*LO Mode, Into a 50 Ω Load, LO Buffer Enabled		3		dBm
LO Input Level	Externally Applied 2XLO, PLL Disabled		0		dBm
LO Input Impedance	Externally Applied 2XLO, PLL Disabled		50		Ω
BASEBAND INPUTS	Pins IBBP, IBBN, QBBP, QBBN				
I and Q Input Bias Level			500		mV
Bandwidth					
3 dB			500		MHz
Input Impedance			1||1		kΩ||pF
SYNTHESIZER SPECIFICATIONS	Synthesizer Specifications Referenced to the Modulator Output.				
Channel Spacing	F_{PFD} = 38.4 MHz,		25		KHz
	F_{PFD} = 38.4 MHz,		20		KHz
Reference Spurs	F_{REF}= 153.6 MHz, F_{PFD} = 38.4 MHz				
	Offset = F_{PFD}		-90		
	Offset = 2xF_{PFD}		-95		dBc
	Offset = 3xF_{PFD}		-92		dBc
	Offset = 4XF_{PFD}		-102		
HARMONICS	2nd Harmonic		-26		dBc
	3rd Harmonic		-16		dBc
PHASE NOISE	Frequency = 2100to 2600 MHz, PFD Frequency= 38.4 MHz or 38.4 MHz				
	@ 1 kHz offset		-93		dBc/Hz
	@ 10 kHz offset		-103		dBc/Hz
	@ 100 kHz offset		-103		dBc/Hz
	@ 1 MHz offset		-129		dBc/Hz
	@ 10 MHz offset		-148		dBc/Hz
	@ 20 MHz offset		-150		dBc/Hz
Normalized In-Band Phase Noise Floor			TBD		dBc/Hz
Integrated Phase Noise	1 KHz to 40 MHz integration bandwidth		0.3		°rms

Parameter	Conditions	Min	Typ	Max	Unit
Frequency Settling	Residual Phase Error = 10°		1		ms
REFERENCE CHARACTERISTICS	REFIN, MUXOUT				
REFIN Input Level	Re: 50 Ω		+4		dBm
REFIN Input Frequency		12		160	MHz
Phase Detector Frequency		21.85	38.4	40	MHz
REFIN Input Capacitance			4		pF
REFIN Input Current				±100	µA
MUXOUT Output Level	V_{OL} (lock detect output selected)			0.25	V
	V_{OH} (lock detect output selected)	2.7			V
MUXOUT Duty Cycle			50		%
CHARGE PUMP					
Pump Current	Programmable: 250uA,500uA,750uA,1000uA		500		uA
Output Compliance Range		1		2.8	Volts
LOGIC INPUTS	CLK, DATA, LE				
Input High Voltage, V_{INH}		1.4		3.3	V
Input Low Voltage, V_{INL}		0		0.7	V
Input Current, I_{INH}/I_{INL},			±0.1		µA
Input Capacitance, C_{IN}			5		pF
POWER SUPPLIES	Pins VDD				
Voltage Range		4.75	5	5.25	V
Supply Current	PLL only		80		mA
	Normal Tx Mode		210		mA
	Tx Mode with LO Buffer Enabled		260		mA
	Power Down Mode		100		uA

TIMING CHARACTERISTICS

Table 3. Serial Interface Timing, V_{CC} = 5 V ± 5%

Parameter	Limit	Unit	Test Conditions/Comments
t_1	20	ns minimum	LE setup time
t_2	10	ns minimum	DATA to CLK setup time
t_3	10	ns minimum	DATA to CLK hold time
t_4	25	ns minimum	CLK high duration
t_5	25	ns minimum	CLK low duration
t_6	10	ns minimum	CLK to LE setup time
t_7	20	ns minimum	LE pulse width

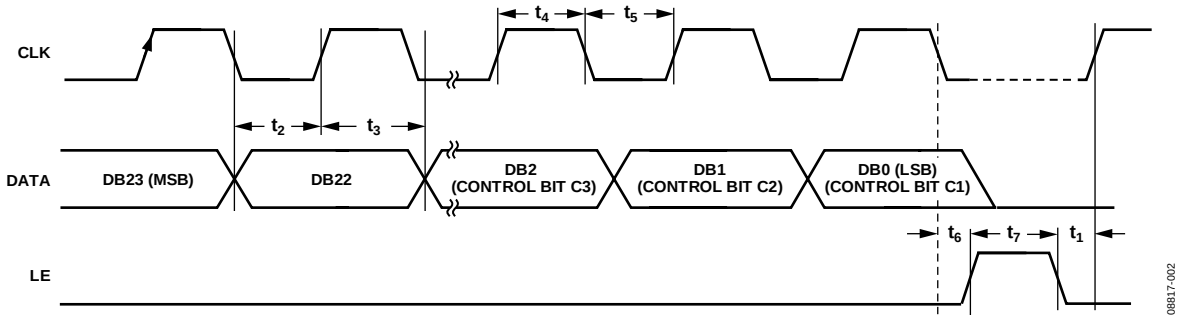

Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage, V_{CC}	5.5 V
Digital I/O CLK, DATA, LE	−0.3 V to +3.6 V
OUTP, OUTN	V_{CC}
LOP, LON	16 dBm
IN, IP, QN, QP	20 dBm
θ_{JA} (Exposed Paddle Soldered Down)	35°C/W
Maximum Junction Temperature	150°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTIONAL DESCRIPTIONS

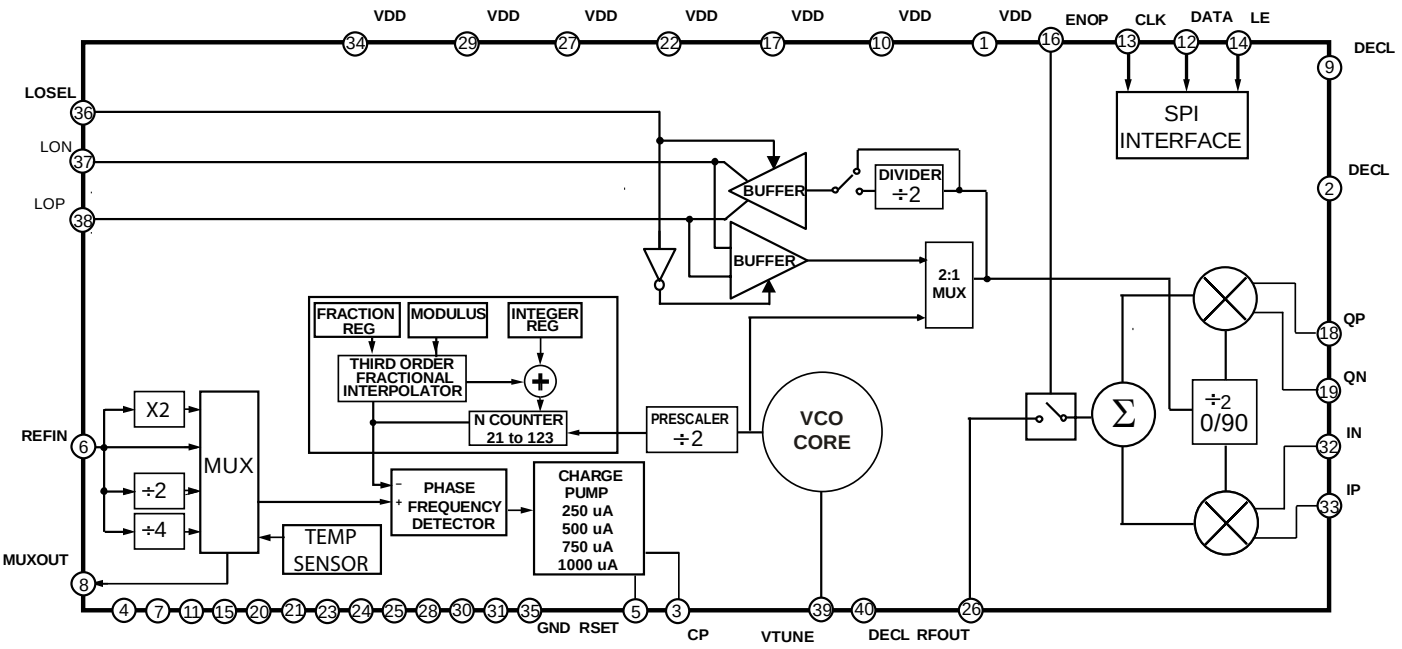

Figure 3. Block Diagram

Table 5. Pin Function Descriptions

Pin Nr.	Mnemonic	Description
1,10,17,22, 27,29,34	VDD	**Power Supply**: Power supply voltage range is 4.75 V to 5.25 V. Each pin should be decoupled with a 100 pf and 0.1uF capacitors located close to the pin.
2,9, 40	DECL	**Internal Decoupling Nodes**: Connect a 100 pF and a 0.1uF capacitor between each of these pins and ground. 10uF capacitors should also be connected to DECL pins 9 and 40.
3	CP	**Charge Pump**: Chargepump Output Pin. Connect to V_{TUNE} through loop filter
4, 7,11,15,20, 21,23,24,25, 28,30,31,35	GND	**Ground**: Connect these pins to a low impedance ground planeGND
5	R_{SET}	**Charge Pump Current**: The nominal charge pump current can be set to either 250 uA, 500 uA, 750 uA or 1 mA using DB10 and DB11 of Register 4 and by setting DB18 to 0 (Internal Reference Current). In this mode, no external R_{SET} is required. If DB18 is set to 1, the four nominal charge pump currents ($I_{NOMINAL}$) can be externally tweaked according to the equation. $$R_{SET}\,[\Omega] = \left[\frac{217.4 \times I_{CP,BASE}}{250}\right] - 37.8$$ Where $I_{CP,BASE}$ is the base charge pump current in µA. For further details on the charge pump current, see Register 4 - Charge Pump, PFD and Reference Path Control.
6	REFIN	**Refence Input**: Nominal input level is 1 V p-p or +4 dBm with the recommended external 50 ohm termination resistor. Input range is 10 MHz to 160 MHz. This pin must be ac-coupled.
8	MUXOUT	**Multiplexer Output**: This output allows either a digital lock detect, a voltage proportional to temperature, or a buffered, frequency-scaled reference signal to be accessed externally. The output is selected by programming the appropriate bits in Register 4.
12	DATA	**Serial Data Input**: The serial data input is loaded MSB first with the three LSBs being the control bits.
13	CLK	**Serial Clock Input**: This serial clock input is used to clock in the serial data to the registers. The data is latched into the 24-bit shift register on the CLK rising edge. Maximum clock frequency is 20 MHz.
14	LE	**Load Enable**: When the LE input pin goes high, the data stored in the shift registers is loaded into one of the six registers, the relevant latch being selected by the first three control bits of the 24-bit word.

<table>
<tr><th>Pin Nr.</th><th>Mnemonic</th><th>Description</th></tr>
<tr><td>16</td><td>ENOP</td><td>Modulator Output Enable/Disable
<table>
<tr><th>ENOP</th><th>R5:DB6</th><th>Output</th></tr>
<tr><td>X</td><td>0</td><td>DISABLED</td></tr>
<tr><td>0</td><td>X</td><td>DISABLED</td></tr>
<tr><td>1</td><td>1</td><td>ENABLED</td></tr>
</table></td></tr>
<tr><td>18,19, 32,33</td><td>QP, QN, IN, IP</td><td>Modulator Baseband Inputs: Differential In-Phase and Quadrature Baseband Inputs. These high impedance inputs should be dc-biased to 0.5 V.</td></tr>
<tr><td>26</td><td>RFOUT</td><td>RF Output: Single-ended, 50 Ω internally biased RF output. RFOUT must be ac-coupled to its load.</td></tr>
<tr><td>36</td><td>LOSEL</td><td>LO Select: This digital input pin determines whether the LOP and LON pins operate as inputs or outputs. LOP and LON become inputs if the LOSEL pin is set low AND the LDRV bit of Register 5 is set low. External LO drive must be a 2XLO. In addition to setting LOSEL and LDRV low and providing an external 2XLO, the LXL bit of Register 5 (DB4) must be set to 1 to direct the external LO to the IQ Modulator. LON and LOP become outputs when LOSEL is high OR if the LDRV bit of Register 5 (DB3) is set high. A 1X or 2X LO output can be selected by setting the LDIV bit of Register 5 (DB5) to 1 or 0 respectively.
<table>
<tr><th>LON/LOP Function</th><th>LOSEL</th><th>R5:DB3 (LDRV)</th><th>R5:DB5(LDIV)</th><th>R5:DB4(LXL)</th></tr>
<tr><td>Input (2XLO)</td><td>0</td><td>0</td><td>X</td><td>1</td></tr>
<tr><td>Output (1XLO)</td><td>X</td><td>1</td><td>0</td><td>X</td></tr>
<tr><td>Output (1XLO)</td><td>1</td><td>X</td><td>0</td><td>X</td></tr>
<tr><td>Output (2XLO)</td><td>X</td><td>1</td><td>1</td><td>X</td></tr>
<tr><td>Output (2XLO)</td><td>1</td><td>X</td><td>1</td><td>X</td></tr>
</table>
X = Don't Care
LOSEL should not be left floating.</td></tr>
<tr><td>37,38</td><td>LON, LOP</td><td>Local Oscillator Input/Output: The internally generated 1XLO or 2XLO is available on these pins.
When internal LO generation is disabled (see LOSEL pin) an external 2XLO can be applied to these pins.</td></tr>
<tr><td>39</td><td>VTUNE</td><td>VCO Control Voltage Input: This pin is driven by the output of the loop filter. Nominal input voltage range on this pin is 1.5 V to 2.5 V</td></tr>
<tr><td></td><td>EP</td><td>Exposed Paddle: The exposed paddle should be soldered to a low impedance ground plane.</td></tr>
</table>

THEORY OF OPERATION

The ADRF6703 integrates a high performance IQ modulator with a state of the art fractional-N PLL. The PLL also integrates a low noise VCO. The programmable SPI port allows the user to control the fractional-N PLL functions and the modulator optimization functions as well as allowing for an externally applied LO or VCO.

The quadrature modulator core within the ADRF670X family is the next generation of industry leading family of modulators from Analog Devices. The baseband inputs are converted to currents and then mixed to RF using high-performance NPN transistors. The mixer output currents are transformed to a single-ended RF output using an integrated RF transformer balun. The high performance active mixer core, coupled with the low-loss RF transformer balun results in an exceptional OIP3 and OP1dB, with a very low output noise floor for excellent dynamic range. The use of a passive transformer balun rather than an active output stage leads to an improvement in OIP3 with no sacrifice in noise floor

The fractional divide function of the PLL allows the frequency multiplication value from REFIN to LO Out to be a fractional value rather than restricted to an integer as in traditional PLLs. In operation, this multiplication value is INT+(FRAC/MOD) where INT is the integer value, FRAC is the fractional value and MOD is the modulus value, all programmable via the SPI port. In previous frac-N PLL designs, the fractional multiplication was achieved by periodically changing the fractional value in a deterministic way. The down side of this was often spurious components close to the fundamental signal. In the ADRF6703, a sigma-delta modulator is used to distribute the fractional value randomly, thus significantly reducing the spurious content due to the fractional function.

BASIC CONNECTIONS

The device's seven power supply pins should be individually decoupled using 100 pF and 0.1 µF capacitors located as close as possible to the device. In additional, internal decoupling nodes (labeled DECL) should be decoupled with the capacitor values shown.

The four IQ inputs should be driven with a bias level of 500 mV. The I and Q inputs are high impedance and should normally be terminated with resistors to provide an appropriate match to the baseband filter which immediately precedes the IQ modulator in the signal chain.

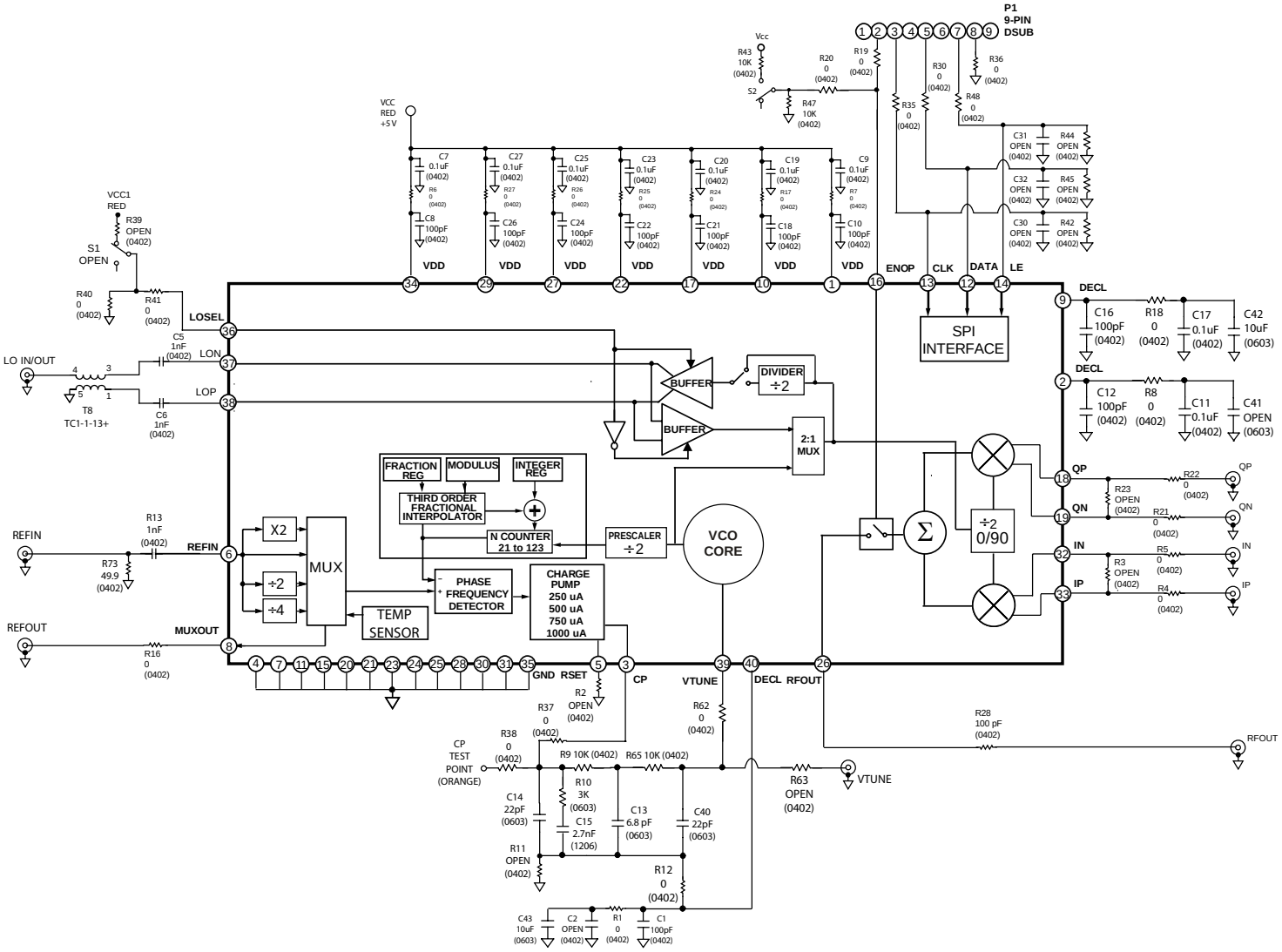

Figure 4. Basic Connections for Operation

PROGRAMMING THE ADRF6703

The ADRF6703 is programmed via a 3-pin SPI port. The timing requirements for the SPI port are shown in Figure 2. Programmable registers, each with 24 bits, control the operation of the device. The register functions are listed in Table 1.

Table 1. ADRF6703 Register Functions

Register	Function
Register 0	Integer divide control for the PLL
Register 1	Modulus divide control for the PLL
Register 2	Fractional divide control for the PLL
Register 3	Σ-Δ modulator dither control
Register 4	PLL charge pump, PFD, reference path control
Register 5	PLL enable and LO path control
Register 6	VCO control and VCO enable
Register 7	Mixer bias enable and external VCO enable

Note that internal calibration for the PLL must be run when the ADRF6703 is initialized at a given frequency. This calibration is run automatically whenever Register 0, Register 1, or Register 2 is programmed. Because the other registers affect PLL performance, Register 0, Register 1, and Register 2 should always be programmed last and in this order: Register 0, Register 1, Register 2.

To program the frequency of the ADRF6703, the user typically programs only Register 0, Register 1, and Register 2. However, if registers other than these are programmed first, a short delay should be inserted before programming Register 0. This delay ensures that the VCO band calibration has sufficient time to complete before the final band calibration for Register 0 is initiated.

Software is available on the product page of the Analog Devices website (www.analog.com) that allows easy programming from a PC running Windows XP or Vista.

INITIALIZATION SEQUENCE

In order to ensure proper power-up of the ADRF6703, it is important to reset the PLL circuitry after the VCC supply rail has settled to 5V +/- 0.25V. Resetting the PLL ensures that the internal bias cells are properly configured even under poor supply start-up conditions. To ensure that the PLL is reset after power-up the L3EN data bit (DB19) and LVEN data bit (DB18) in register 6 should be programmed to disable the PLL (L3EN=0, LVEN=0). After a delay of >100ms, register 6 should be programmed to enable the PLL (L3EN=1, LVEN=1). After this procedure, the registers should be programmed as indicated below:

Register 7
Register 6
Register 4
Register 3
Register 2
Register 1
Delay >1ms
Register 0

REGISTER 0 INTEGER DIVIDE CONTROL

With R0[2:0] set to 000, the on-chip integer divide control register is programmed as shown in figure 39.

INTEGER DIVIDE RATIO

The integer divide ratio is used to set the INT value in Equation 1. The INT, FRAC, and MOD values make it possible to generate output frequencies that are spaced by fractions of the PFD frequency. The VCO frequency (F_{VCO}) equation is:

$$F_{VCO} = 2 \times f_{PFD} \times (INT + (FRAC/MOD)) \quad (1)$$

Where:
F_{VCO} is the output frequency of the internal VCO.
INT is the preset integer divide ratio value (24 to 119 in fractional mode).
MOD is the preset fractional modulus (1 to 2047).
FRAC is the preset fractional divider ratio value (0 to MOD-1).

DIVIDE MODE

Divide mode determines whether fractional mode or integer mode is used. In integer mode, the RF VCO output frequency (F_{VCO}) is calculated using the following equation:

$$F_{VCO} = 2 \times f_{PFD} \times (INT) \quad (2)$$

where INT is the integer divide ratio value (21 to 123 in integer mode).

													Divide Mode	Integer Divide Ratio								Control Bits	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	0	0	0	DM	ID6	ID5	ID4	ID3	ID2	ID1	ID0	C3(0)	C2(0)	C1(0)

DM	Divide Mode
0	Fractional (default)
1	Integer

ID6	ID5	ID4	ID3	ID2	ID1	ID0	Divide Ratio
0	0	1	0	1	0	1	21 (Integer mode only)
0	0	1	0	1	1	0	22 (Integer mode only)
0	0	1	0	1	1	1	23 (Integer mode only)
0	0	1	1	0	0	0	24
-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-
0	1	1	1	0	0	0	56 (default)
-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-
1	1	1	0	1	1	1	119
1	1	1	1	0	0	0	120 (Integer mode only)
1	1	1	1	0	0	1	121 (Integer mode only)
1	1	1	1	0	1	0	122 (Integer mode only)
1	1	1	1	0	1	1	123 (Integer mode only)

Figure 5. Integer Divide Control Register (R0)

										Modulus Divide Ratio											Control Bits		
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	MD10	MD9	MD8	MD7	MD6	MD5	MD4	MD3	MD2	MD1	MD0	C3(0)	C2(0)	C1(1)

MD10	MD9	MD8	MD7	MD6	MD5	MD4	MD3	MD2	MD1	MD0	Modulus
0	0	0	0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	0	0	0	1	0	2
-	-	-	-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-	-
0	0	0	0	1	1	0	0	0	0	0	1536 (default)
-	-	-	-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-	-
1	1	1	1	1	1	1	1	1	1	1	2047

Figure 6. Modulus Divide Control Register (R1)

REGISTER 1—MODULUS DIVIDE CONTROL

With R1[2:0] set to 001, the on-chip modulus divide control register is programmed as shown in figure 40.

The MOD value is the preset fractional modulus ranging from 1 to 2047.

										Fractional Divide Ratio											Control Bits		
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	FD10	FD9	FD8	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0	C3(0)	C2(1)	C1(0)

FD10	FD9	FD8	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0	Fractional Value
0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	1	1
-	-	-	-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-	-
0	1	1	0	0	0	0	0	0	0	0	768 (default)
-	-	-	-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-	-
Fractional Value must be less than Modulus											<MDR

Figure 7. Fractional Divide Control Register (R2)

REGISTER 2—FRACTIONAL DIVIDE CONTROL

With R2[2:0] set to 010, the on-chip fractional divide control register is programmed as shown in figure 41.

The FRAC value is the preset fractional modulus ranging from 0 to MOD-1.

	Dither Magnitude		Dither Enable	Dither Restart Value																	Control Bits		
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	DITH1	DITH0	DEN	DV16	DV15	DV14	DV13	DV12	DV11	DV10	DV9	DV8	DV7	DV6	DV5	DV4	DV3	DV2	DV1	DV0	C3(0)	C2(1)	C1(1)

DEN	Dither Enable
0	Disable
1	Enable (default, recommended)

DITH1	DITH0	Dither Magnitude
0	0	15 (default)
0	1	7
1	0	3
1	1	1 (recommended)

DV16	DV15	DV14	DV13	DV12	DV11	DV10	DV9	DV8	DV7	DV6	DV5	DV4	DV3	DV2	DV1	DV0	Dither Restart Value
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0x00001 (default)
'	'	'	'	'	'	'	'	'	'	'	'	'	'	'	'	'	'
'	'	'	'	'	'	'	'	'	'	'	'	'	'	'	'	'	'
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0x1FFFF

Figure 8. Sigma Delta Modulator Dither Control Register (R3)

REGISTER 3—SIGMA DELTA MODULATOR DITHER CONTROL

With R3[2:0] set to 011, the on-chip sigma delta modulator dither control register is programmed as shown in figure 42.

The dither restart value can be programmed from 0 to 2^{17}-1, though a value of 1 is typically recommended.

REGISTER 4—CHARGE PUMP, PFD AND REFERENCE PATH CONTROL

With R4[2:0] set to 100, the on-chip Charge Pump, PFD and Reference Path Control register is programmed as shown in figure 43.

The charge pump current is controlled by the base charge pump current ($I_{CP,BASE}$), and the value of the charge pump current multiplier ($I_{CP,MULT}$).

The base charge pump current can be set using an internal or external resistor (according to DB18 of Register 4). When using an external resistor, the value of $I_{CP,BASE}$ can be varied according to the following table.

$$R_{SET}\ [\Omega] = \left[\frac{217.4 \times I_{CP,BASE}}{250}\right] - 37.8$$

The actual charge pump current can be programmed to be a multiple (1, 2, 3, 4) of the charge pump base current. The multiplying value ($I_{CP,MULT}$) is equal to 1 plus the value of bits DB11 and DB10 in register 4.

The PFD phase offset multiplier ($\theta_{PFD,OFS}$), which is set by bits DB16-DB12 of Register 4, will cause the PLL to lock with a nominally fixed phase offset between the PFD reference signal and the divided-down VCO signal. This phase offset is used to linearize the PFD-CP transfer function and can improve fractional spurs. The magnitude of the phase offset is determined by the following equation:

$$|\Delta\Phi|[\text{deg}] = 22.5\frac{\theta_{PFD,OFS}}{I_{CP,MULT}}$$

Finally, the phase offset can be either positive or negative depending on the value of DB17 in register 4.

The reference frequency applied to the PFD can be manipulated using the internal reference path source. The external reference frequency applied can be internally scaled in frequency by 2X, 1X, 0.5X, or 0.25X. This allows a broader range of reference frequency selections while keeping the reference frequency applied to the PFD within an acceptable range.

The ADRF6655 also provides a MUXOUT pin that can be programmed to output a selection of several internal signals. The default mode is to provide a lock-detect output to allow the user to verify when the PLL has locked to the target frequency. In addition, several other internal signals may be passed to the MUXOUT pin as described in figure 43.

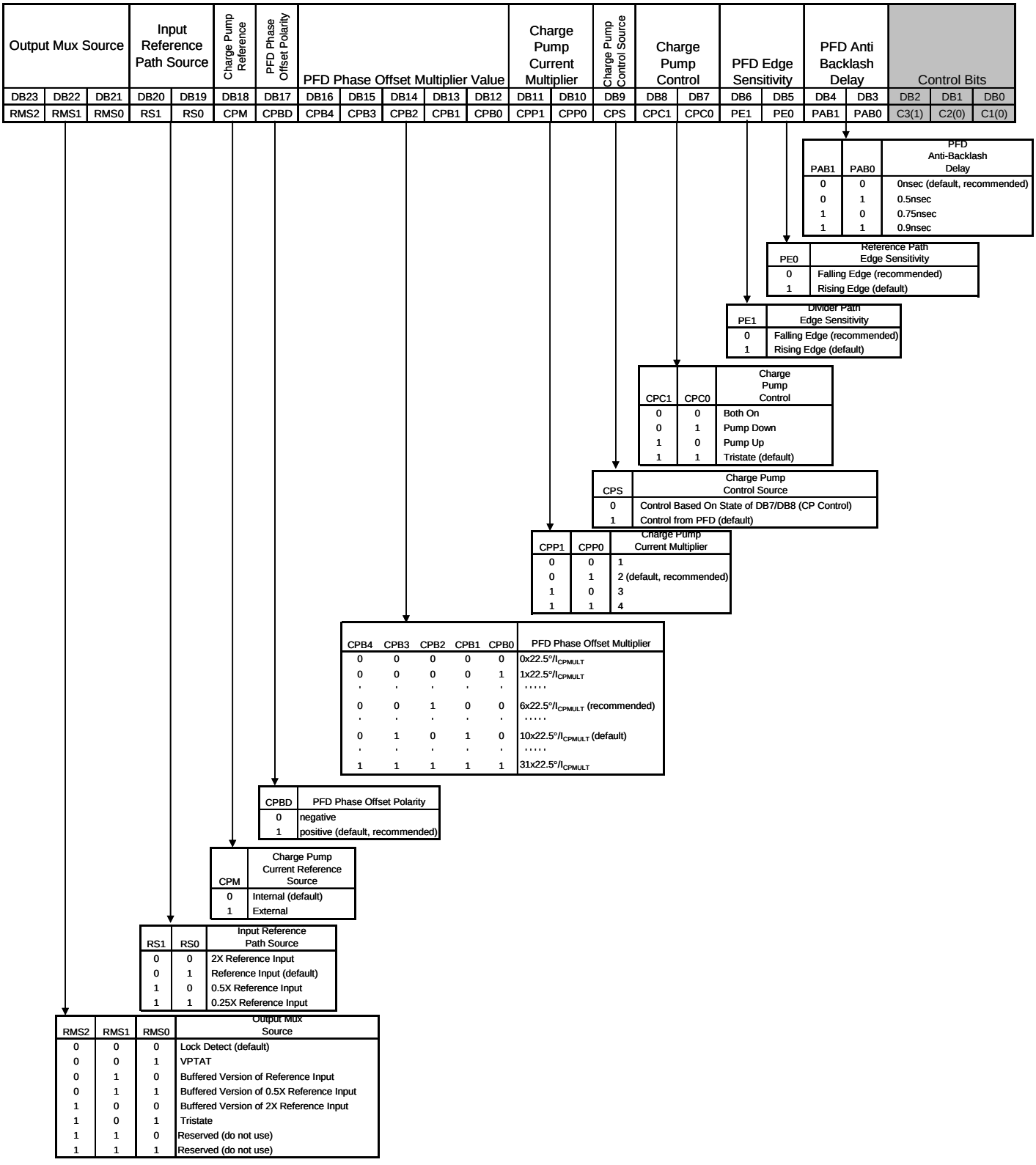

Figure 9. Charge Pump, PFD, and Reference Path Control Register (R4)

REGISTER 5 LO PATH AND MODULATOR CONTROL

The modulator output or the complete modulator can be disabled using the modulator bias enable and modulator output enable addresses of register 5.

The LO port (pins LOP and LON) can be used to apply an external 2X LO (i.e. bypass internal PLL) to the IQ Modulator. A differential LO drive of 0 dBm is recommended for best LO suppression at the RF output. When using an external frequency stable local oscillator signal to commutate the mixer core it is possible to shut down the PLL circuitry through the PLL enable address of register 5.

The LO port can also be used as an output where a 2X or 1X LO can be brought out and used to drive another mixer. The nominial output power provided at the LO port is +3 dBm.

The LO port's mode of operation is determined by the status of the LOSEL pin (3.3 V logic) along with the settings in a number of internal registers.

Table 6. LO Port Configuration

LON/LOP Function	LOSEL	R5:DB3 (LDRV)	R5:DB5 (LDIV)	R5:DB4(LXL)
Input (2XLO)	0	0	X	1
Output (1XLO)	X	1	0	X
Output (1XLO)	1	X	0	X
Output (2XLO)	X	1	1	X
Output (2XLO)	1	X	1	X

X = Don't Care

The device's internal VCO can also be bypassed. In this case, the charge pump output drives an external VCO through the loop filter. The loop is completed by routing the VCO in to the device through the LO Port.

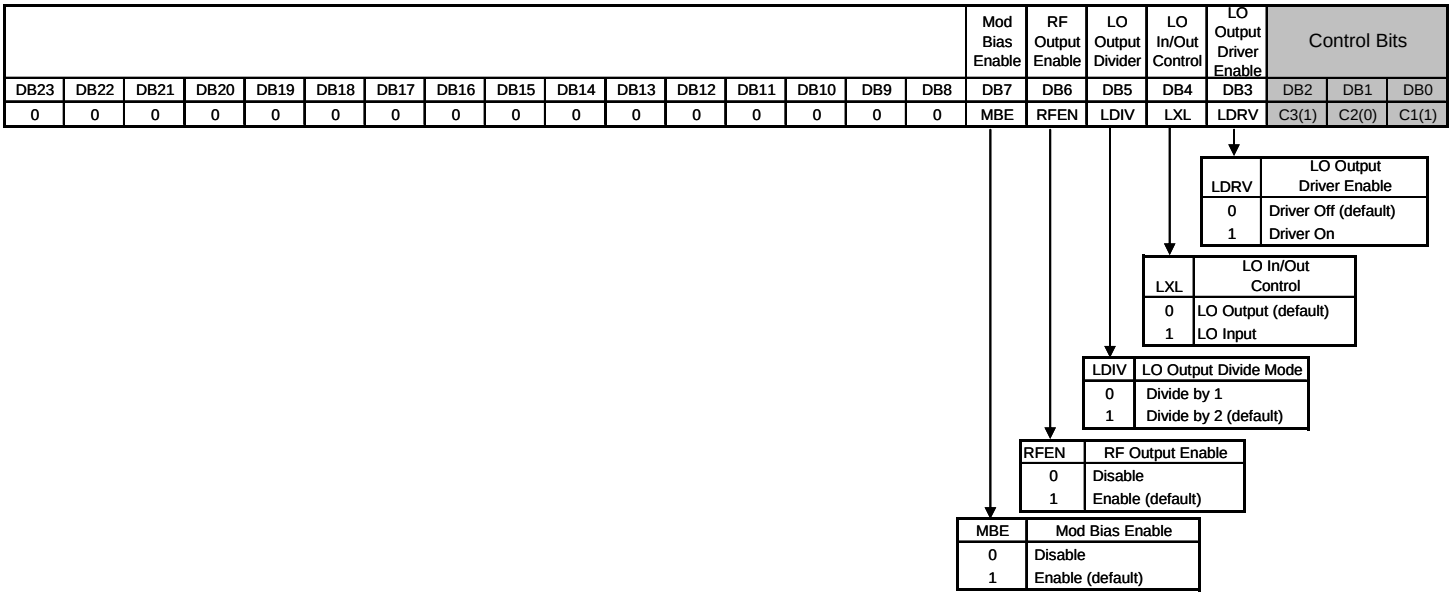

Figure 10. LO Path and Modulator Control (R5)

REGISTER 6 VCO CONTROL AND ENABLES

With R6[2:0] set to 110, the VCO Control and Enables register is programmed as shown in figure 16.

VCO band selection is normally selected based on BANDCAL calibration, though the user can directly select the VCO band using register 6. The VCO BS SRC determines whether the BANDCAL calibration will determine the optimum VCO tuning band, or if the external SPI interface will be used to select the VCO tuning band based on the value of the VCO Band Select.

The VCO amplitude can be controlled through register 6. The VCO amplitude setting can be controlled between 0 and 31 decimal, with a default value of 31.

The internal VCO can be disabled using register 6. The internal VCO LDO can be disabled if an external clean 2.5V supply is available to be applied to pins 9 and 16. Additionally the 3.3V on-board LDO can be disabled through register 6 and an external 3.3V supply can be applied to pin 2.

The internal charge pump can be disabled through register 6. Normally the charge pump will be enabled.

			Charge Pump Enable	LDO 3.3V Enable	VCO LDO Enable	VCO Enable	VCO Switch Control	VCO Amplitude Setting						VCO BS SRC	VCO Band Select						Control Bits		
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	CPEN	L3EN	LVEN	VCOEN	VCOSW	VC5	VC4	VC3	VC2	VC1	VC0	VBSRC	VBS5	VBS4	VBS3	VBS2	VBS1	VBS0	C3(1)	C2(1)	C1(0)

VBS5	VBS4	VBS3	VBS2	VBS1	VBS0	VCO Band Select from SPI
0	0	0	0	0	0	0
'	'	'	'	'	'	' ' ' ' ' '
1	0	0	0	0	0	32 (default)
'	'	'	'	'	'	' ' ' ' ' '
1	1	1	1	1	1	47

VBSRC	VCO Band Calibration & SW Source Control
0	BANDCAL (default)
1	SPI

VC5	VC4	VC3	VC2	VC1	VC0	VCO Amplitude Setting
0	0	0	0	0	0	0
'	'	'	'	'	'	' ' ' ' ' '
1	1	1	1	1	1	63 (recommended)

VCOSW	VCO Switch Control from SPI
0	Regular (default)
1	BANDCAL

VCOEN	VCO Enable
0	Disable
1	Enable (default)

LVEN	VCO LDO Enable
0	Disable
1	Enable (default)

L3EN	3.3V LDO Enable
0	Disable
1	Enable (default)

CPEN	Charge Pump Enable
0	Disable
1	Enable (default)

Figure 11. VCO Control and Enable(R6)

REGISTER 7 EXTERNAL VCO ENABLE

With R6[2:0] set to 111, the External VCO Control register is programmed as shown in figure 9.

The External VCO Enable bit allows the use of an external VCO in the PLL instead of the internal VCO. This can be advantageous in cases where the internal VCO is not capable of providing the desired frequency or where the internal VCO's phase noise is higher than desired. By setting this bit (DB22) to 1, and setting Register 6, bits DB15-DB10 to 0, the internal VCO is disabled, and the output of an external VCO can be fed into the part differentially on pins 38,37 (LOP,LON). Since the loop filter is already external, the output of the loop filter simply needs to be connected to the external VCO's tuning voltage pin.

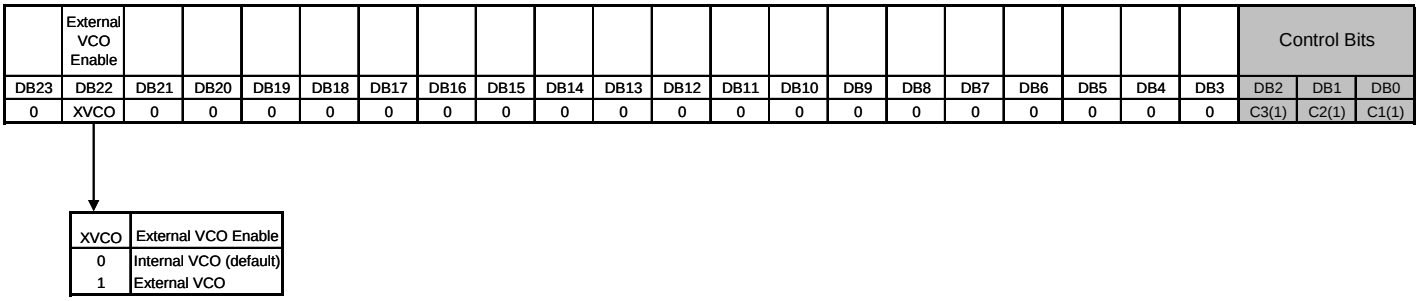

Figure 12. VCO Control and Enable (R7)

OUTLINE DIMENSIONS

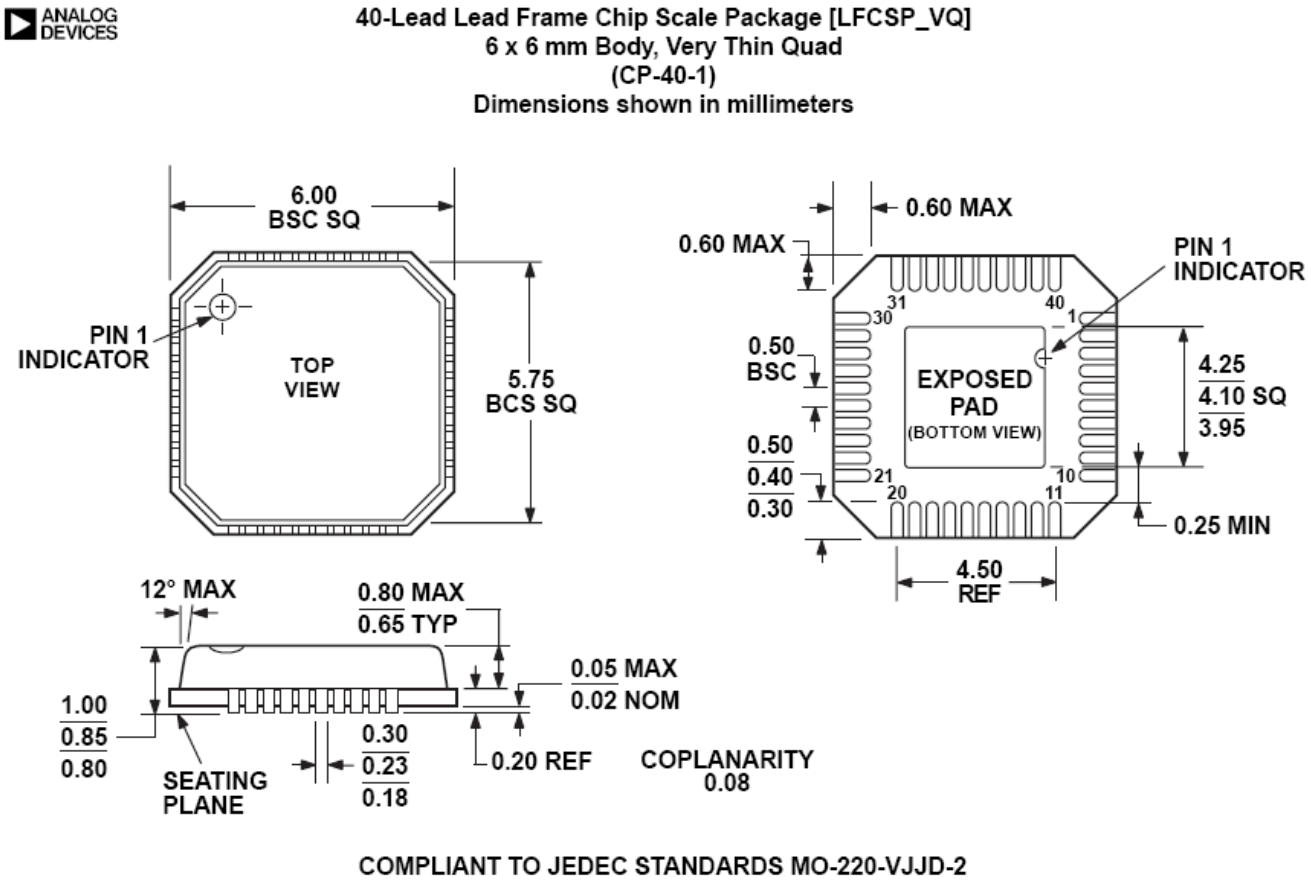

Figure 13. 40-Lead LFCSP with exposed paddle.

Table 7. Ordering Guide

Model	Temperature Range (°C)	Package Description	Package Option
ADRF6703ACPZ[1]	-40 to +85	40-Lead Lead Frame Chip Scale Package	
ADRF6703-EVALZ		Evaluation Board	

[1] Z = RoHS Compliant Part